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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2008*.
2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-41* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *28 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All   b)☐ Some *   c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date *1/30/08 & 1/31/08*.
4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

1.   This communication is in response to the Applicants' amendment mailed on April

14, 2008. Claims 7, 18, 27 and 36 were amended. Claims 1-41 of the application are

pending. This office action is made non-final.

Claim Rejections - 35 USC § 101

2.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or
> any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and
> requirements of this title.

3.   Claims 1-12 are rejected under 35 U.S.C. 101 because the claimed inventions are directed

to non-statutory subject matter.

3.1   Claim 1 states in the preamble, "A method of simulating an operation of a logical unit".

The method comprises mental steps of requesting a resource to a resource manager, allocating a

resource to said thread and controlling an execution state of said thread, said thread manager and

said resource manager executing said requesting, allocating, and controlling repeatedly until the

execution of said thread reaches completion. The method is not tied to a statutory hardware

device or apparatus and is not implemented in a computer. A method comprising only mental

steps not implemented in a hardware or apparatus or a computer cannot be patented under 35

USC 101.

Claims 2-12 depend on claim 1, but include only mental steps of a method, that is not tied

to any statutory hardware and is not implemented in a computing device. Therefore, these

claims cannot be patented under 35 USC 101.

Claim Interpretation

4.   The applicants have explained in their amendment on Page 14, Para 2 that resource

signifies "information about a hardware resource" as disclosed in the specification on Page 22,

Lines 8-11. The Examiner has used this interpretation of the "information about hardware

resource" to mean same as "the resource" in all art rejections that follow.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

6.   Claims 1-7, 10-18, 21-27, 30-36 and 39-41 are rejected under 35 U.S.C. 103(a) as being

unpatentable over **Emer et al.** (U.S. Patent 6,493,741) in view of **Stamm et al.** (U.S. Patent

6,711,616).

6.1   **Emer et al.** teaches method and apparatus to quiesce a portion of a simultaneous multi-

threaded central processing unit. Specifically as per claim 1, **Emer et al.** teaches a method of

simulating an operation of a logical unit (CL2, L16-21; CL5, L22-25); comprising:

a thread manager, which controls threads each forming an execution unit of a program,

for execution of each of threads representative of a series of functions required until the

operation of the logical unit reaches completion according to a design specification of the logical

unit (Fig. 2; Fig. 3, Item 305; CL1, L7-21; Fig. 1(c); CL1, L66 to CL2, L3; CL2, L16-21);

requesting a resource in which a thread manager makes a request for information about a

hardware resource relating to a hardware resource needed for execution of each of threads, to a

resource manager which manages the information about the hardware resource (CL2, L3-6:

Emer states at CL2, L3-6 that SMT processor selects instructions for execution from all threads;

and the processor then dynamically schedules machine resources among the instruction. The

examiner interprets this to mean that a thread manager makes a request for information about a

hardware resource and allocating information about a hardware resource relating to necessary

hardware resources to the thread by a resource manager);

allocating a resource in which the resource manager allocates the information about a

hardware resource meeting the request to the thread (CL2, L3-6: Emer states at CL2, L3-6 that

SMT processor selects instructions for execution from all threads; and the processor then

dynamically schedules machine resources among the instruction. The examiner interprets this to

mean that a thread manager makes a request for information about a hardware resource and

allocating information about a hardware resource relating to necessary hardware resources to the

thread by a resource manager);

controlling a thread in which the thread manager controls an execution state of the thread

in accordance with a result of the allocation made by the resource manager (CL1, L10-21; Fig. 1

(c); CL1, L66 to CL2, L6); and

dynamically allocating information about a hardware resource relating to necessary

hardware resources to the thread by the resource manager every time the generated thread is

executed (CL2, L3-6: Emer states at CL2, L3-6 that SMT processor selects instructions for

execution from all threads; and the processor then dynamically schedules machine resources

among the instruction. The examiner interprets this to mean that a thread manager makes a

request for information about a hardware resource and allocating information about a hardware

resource relating to necessary hardware resources to the thread by a resource manager).

Emer et al. does not expressly teach allocating a resource in which the resource manager

allocates the information about a hardware resource meeting the request to the thread in

accordance with a rule prescribed in advance. **Stamm et al.** teaches allocating a resource in

which the resource manager allocates the information about a hardware resource meeting the

request to the thread in accordance with a rule prescribed in advance (CL1, L23-25 and 28-30;

CL1, L51-62; Abstract, L8-11; CL4, L11-16; CL4, L36-38; CL6, L1-5). It would have been

obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the

method of **Emer et al.** with the method of **Stamm et al.** that included allocating a resource in

which the resource manager allocates the information about a hardware resource meeting the

request to the thread in accordance with a rule prescribed in advance because that would allow

selecting a thread for execution by the processor as a function of resource requirements of the

thread and the available resource characteristics of the processor (Abstract, L8-11); such that the

resource requirements of the thread most closely matched the available resources of the

processor (CL4, L11-15); and defining a hierarchy of threads to be executed, defining an

allocation of resources among the threads and selecting the threads based on the criteria

previously described (CL6, L1-5).

Emer et al. teaches the thread manager and the resource manager executing the

requesting, allocating, and controlling in cooperation with each other until the execution of the

thread reaches completion simulating the operation of the logical unit to be conducted up to the

completion (CL1, L10-21; Fig. 1 (c); CL1, L66 to CL2, L6). **Emer et al.** does not expressly

teach the thread manager and the resource manager executing the requesting, allocating, and

controlling repeatedly in cooperation with each other until the execution of the thread reaches

completion simulating the operation of the logical unit to be conducted up to the completion.

Stamm et al. teaches the thread manager and the resource manager executing the requesting,

allocating, and controlling repeatedly in cooperation with each other until the execution of the

thread reaches completion simulating the operation of the logical unit to be conducted up to the

completion (Abstract; Fig. 3; Fig. 4).

Per claim 2: **Emer et al.** does not expressly teach that the series of functions are

represented in a plurality of sequential threads. **Stamm et al.** teaches that the series of functions

are represented in a plurality of sequential threads (CL2, L39-48).

Per claim 3: **Emer et al.** teaches that the series of functions are represented in a plurality

of concurrently executed threads (CL1, L10-12). **Emer et al.** does not expressly teach that the

series of functions are represented in a plurality of sequential threads. **Stamm et al.** teaches that

the series of functions are represented in a plurality of sequential executed threads (CL2, L39-

48).

Per claim 4: **Emer et al.** does not expressly teach that a plurality of resource managers

each corresponding to the resource manager are provided in conjunction with the types of the

information about hardware resources, and in the allocating a resource, each of the resource

managers allocates the information about a hardware resource, the resource manager manages, to

the thread in accordance with a local rule described in advance. **Stamm et al.** teaches that a

plurality of resource managers each corresponding to the resource manager are provided in

conjunction with the types of the information about hardware resources (CL1, L23-25 and 28-30;

CL1, L51-62; CL4, L36-38 and 54-55), and in the allocating a resource, the resource manager

allocates the information about a hardware resource, the resource manager manages, to the

thread (CL1, L23-25 and 28-30; CL1, L51-62; CL4, L36-38) in accordance with a local rule

described in advance (CL1, L59-62; Abstract, L8-11; CL4, L11-16; CL4, L36-38; CL6, L1-5).

      Per claim 5: **Emer et al.** does not expressly teach a plurality of resource managers each

corresponding to the resource manager are provided in conjunction with the types of the

information about hardware resources and are hierarchized according to the dependence among

the information about hardware resources, and in the resource allocating, the allocation of

information about a hardware resource is made in consideration of the dependence between the

information about a hardware resource managed by one of the resource managers and the

information about a hardware resource managed by the other resource manager lower in

hierarchy than the one of the resource managers. **Stamm et al.** teaches a plurality of resource

managers each corresponding to the resource manager are provided in conjunction with the types

of the information about hardware resources (CL1, L23-25 and 28-30; CL1, L51-62; CL4, L36-

38 and 54-55) and are hierarchized according to the dependence among the information about

hardware resources (CL3, L8-10; CL4, L43-47; Fig. 5; CL5, L61-67; CL6, L1-5), and in the

resource allocating, the allocation of information about a hardware resource is made in

consideration of the dependence between the information about a hardware resource managed by

one of the resource managers and the information about a hardware resource managed by the

other resource manager lower in hierarchy than the one of the resource managers (CL3, L8-10;

CL4, L43-47; Fig. 5; CL5, L61-67; CL6, L1-5).

Per claim 6: **Emer et al.** teaches that the resource manager monitors resource requests in

the requesting a resource to make a decision on a resource request deadlock state among a

plurality of threads as a result of the monitoring (CL3, L29-35; CL3, L49-55; CL9, L4-13)).

Per claim 7: **Emer et al.** teaches that the resource manager monitors requests with respect

to the information about a hardware resource allocated by the resource manager in the allocating

a resource to make a decision on a competition state in operation on the information about a

hardware resource among a plurality of threads on the basis of a result of the monitoring (CL2,

L37-41; CL2, L44-56; CL3, L43-46).

Per claim 10: **Emer et al.** teaches that the thread has a budget on a time of occupancy of

information about a hardware resource relating to a hardware resource allocated by the resource

manager (CL4, L24-29; CL4, L32-34).

Per claim 11: **Emer et al.** teaches that the thread has an execution time-limit on the

function (CL4, L24-29; CL4, L32-34)..

6.2   As per claim 12, **Emer et al.** teaches a method of simulating an operation of a logical

unit (CL2, L16-21; CL5, L22-25); comprising:

a thread manager, which controls threads each forming an execution unit of a program,

for execution of each of threads representative of a series of functions required until the

operation of the logical unit reaches completion according to a design specification of the logical

unit (Fig. 2; Fig. 3, Item 305; CL1, L7-21; Fig. 1(c); CL1, L66 to CL2, L3; CL2, L16-21);

requesting a resource in which a thread manager makes a request for information about a

hardware resource relating to a hardware resource needed for execution of each of threads, to a

resource manager which manages the information about the hardware resource (CL2, L3-6);

allocating a resource in which the resource manager allocates the information about a

hardware resource meeting the request to the thread (CL2, L3-6);

controlling a thread in which the thread manager controls an execution state of the thread

in accordance with a result of the allocation made by the resource manager (CL1, L10-21; Fig. 1

(c); CL1, L66 to CL2, L6);

dynamically allocating information about a hardware resource relating to necessary

hardware resources to the thread by the resource manager every time the generated thread is

executed (CL2, L3-6);

comparing a result of the simulation with an estimated value on the operation of the

logical unit (CL5, L22-27);

and outputting a result of the comparison to an external unit (CL5, L22-27).

Emer et al. does not expressly teach allocating a resource in which the resource manager

allocates the information about a hardware resource meeting the request to the thread in

accordance with a rule prescribed in advance. **Stamm et al.** teaches allocating a resource in

which the resource manager allocates the information about a hardware resource meeting the

request to the thread in accordance with a rule prescribed in advance (CL1, L23-25 and 28-30;

CL1, L51-62; Abstract, L8-11; CL4, L11-16; CL4, L36-38; CL6, L1-5).

Emer et al. teaches the thread manager and the resource manager executing the

requesting, allocating, and controlling in cooperation with each other until the execution of the

thread reaches completion simulating the operation of the logical unit to be conducted up to the

completion (CL1, L10-21; Fig. 1 (c); CL1, L66 to CL2, L6). **Emer et al.** does not expressly

teach the thread manager and the resource manager executing the requesting, allocating, and

controlling repeatedly in cooperation with each other until the execution of the thread reaches

completion simulating the operation of the logical unit to be conducted up to the completion.

Stamm et al. teaches the thread manager and the resource manager executing the requesting,

allocating, and controlling repeatedly in cooperation with each other until the execution of the

thread reaches completion simulating the operation of the logical unit to be conducted up to the

completion (Abstract; Fig. 3; Fig. 4).

6.3   As per claim 13, **Emer et al.** teaches an apparatus for simulating an operation of a logical

unit (Fig. 2; Fig. 6; CL2, L16-21; CL5, L22-25); comprising:

        a thread manager for controlling a thread forming an execution unit of a program (CL1,

L10-21; Fig. 1 (c); CL1, L66 to CL2, L6);

        a resource manager for managing information about a hardware resource relating to a

hardware resource needed for execution of the thread (CL2, L3-6); the thread manager including:

a thread manager for execution of a thread representative of functions required until the

operation of the logical unit reaches completion according to a design specification of the logical

unit (Fig. 2; Fig. 3, Item 305; CL1, L7-21; Fig. 1(c); CL1, L66 to CL2, L3; CL2, L16-21);

resource requesting means for making a request for information about a hardware

resource relating to a hardware resource needed for execution of a thread to the resource

manager (CL2, L3-6);

thread control means for controlling an execution state of the thread in accordance with a

result of a resource allocation made by the resource manager in response to the request from the

resource requesting means (CL1, L10-21; Fig. 1 (c); CL1, L66 to CL2, L6); the resource

manager including:

resource allocating means for allocating information about a hardware resource relating

to a hardware resource meeting the request to the thread (CL2, L3-6); and

dynamically allocating information about a hardware resource relating to necessary

hardware resources to the thread by the resource manager every time the generated thread is

executed (CL2, L3-6).

Emer et al. does not expressly teach resource allocating means for allocating information

about a hardware resource relating to a hardware resource meeting the request to the thread in

accordance with a rule prescribed in advance. **Stamm et al.** teaches resource allocating means

for allocating information about a hardware resource relating to a hardware resource meeting the

request to the thread in accordance with a rule prescribed in advance (CL1, L23-25 and 28-30;

CL1, L51-62; Abstract, L8-11; CL4, L11-16; CL4, L36-38; CL6, L1-5).

Emer et al. teaches the thread manager and the resource manager conducting the resource request and the control of the thread execution state in cooperation with each other until the execution of the thread reaches completion for simulating the operation of the logical unit to be conducted up to the completion (CL1, L10-21; Fig. 1 (c); CL1, L66 to CL2, L6). **Emer et al.** does not expressly teach the thread manager and the resource manager conducting the resource request and the control of the thread execution state repeatedly in cooperation with each other until the execution of the thread reaches completion for simulating the operation of the logical unit to be conducted up to the completion. **Stamm et al.** teaches the thread manager and the resource manager conducting the resource request and the control of the thread execution state repeatedly in cooperation with each other until the execution of the thread reaches completion for simulating the operation of the logical unit to be conducted up to the completion (Abstract; Fig. 3; Fig. 4).

6.4   As per Claim 14, it is rejected based on the same reasoning as Claim 13, <u>supra.</u> Claim 14 is a computer readable recording medium claim reciting the same limitations as Claim 13, as taught throughout by **Emer et al.** and **Stamm et al.**

6.5   As per Claims 15-22, these are rejected based on the same reasoning as Claims 4-11, <u>supra.</u> Claims 15-22 are a computer readable recording medium claim reciting the same limitations as Claims 4-11, as taught throughout by **Emer et al.** and **Stamm et al.**

6.6   As per Claims 23-31, these are rejected based on the same reasoning as Claims 2 and 4-11, <u>supra.</u> Claims 23-31 are computer readable recording medium claims reciting the same limitations as Claims 2 and 4-11, as taught throughout by **Emer et al.** and **Stamm et al.**

6.7   As per Claims 32-40, these are rejected based on the same reasoning as Claims 3 and 4-11, <u>supra.</u> Claims 32-40 are computer readable recording medium claims reciting the same limitations as Claims 3 and 4-11, as taught throughout by **Emer et al.** and **Stamm et al.**

6.8   As per Claim 41, it is rejected based on the same reasoning as Claim 12, <u>supra.</u> Claim 41 is a computer readable recording medium claim reciting the same limitations as Claim 12, as taught throughout by **Emer et al.** and **Stamm et al.**

7.   Claims 8, 19, 28 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Emer et al.** (U.S. Patent 6,493,741) in view of **Stamm et al.** (U.S. Patent 6,711,616), and further in view of **Chrysos et al.** (U.S. Patent 6,549,930).

7.1   As per claim 8, **Emer et al.** and **Stamm et al.** teach the method of claim 1. **Emer et al.** teaches that the resource manager monitors the number of resource requests with respect to the information about a hardware resource (CL3, L29-35; CL3, L49-55).

        Emer et al. and **Stamm et al.** do not expressly teach that the resource manager monitors the number of resource requests with respect to the information about a hardware resource to detect a bottleneck on the thread on the basis of a result of the monitoring. **Chrysos et al.**

teaches that the resource manager monitors the number of resource requests with respect to the

information about a hardware resource to detect a bottleneck on the thread on the basis of a result

of the monitoring (CL2, L4-8; CL4, L50-55). It would have been obvious to one of ordinary skill

in the art at the time of Applicants' invention to modify the method of **Emer et al.** and **Stamm et**

al. with the method of **Chrysos et al.** that included the resource manager monitoring the number

of resource requests with respect to the information about a hardware resource to detect a

bottleneck on the thread on the basis of a result of the monitoring because that would allow

measuring the resource utilizations of the threads while they were executing and scheduling the

threads according to the measured resource utilizations (Abstract, L2-7), so the computer system

performance could be optimized (CL1, L49-50).

7.2   As per Claims 19, 28 and 37, these are rejected based on the same reasoning as Claim 8,

supra. Claims 19, 28 and 37 are computer readable recording medium claims reciting the same

limitations as Claim 8, as taught throughout by **Emer et al., Stamm et al.** and **Chrysos et al.**

8.   Claims 9, 20, 29 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Emer et al. (U.S. Patent 6,493,741) in view of **Stamm et al.** (U.S. Patent 6,711,616), and further

in view of **Agrawal et al.** (U.S. Patent 5,768,500).

8.1   As per claim 9, **Emer et al.** and **Stamm et al.** teach the method of claim 1. **Emer et al.**

and **Stamm et al.** do not expressly teach that the resource manager monitors the number of

resource requests with respect to the information about a hardware resource to detect blocking of

the resource requests on the basis of a result of the monitoring. **Agrawal et al.** teaches that the

resource manager monitors the number of resource requests with respect to the information about

a hardware resource to detect blocking of the resource requests on the basis of a result of the

monitoring (CL8, L34-45; CL15, L20-25; CL18, L10-32). It would have been obvious to one of

ordinary skill in the art at the time of Applicants' invention to modify the method of **Emer et al.**

and **Stamm et al.** with the method of **Agrawal et al.** that included the resource manager

monitoring the number of resource requests with respect to the information about a hardware

resource to detect blocking of the resource requests on the basis of a result of the monitoring

because that would allow isolating performance bottlenecks and guiding optimization of

architectures, operating systems, compilers and applications (CL2, L52-55).

8.2   As per Claims 20, 29 and 38, these are rejected based on the same reasoning as Claim 9,

supra. Claims 20, 29 and 38 are computer readable recording medium claims reciting the same

limitations as Claim 9, as taught throughout by **Emer et al., Stamm et al.** and **Agrawal et al.**

Response to Arguments

9.   Applicants' arguments filed on April 14, 2008 have been fully considered. Claim

rejections under 35 USC 112 First paragraph are withdrawn in response to applicants'

arguments. Applicants' arguments with respect to claim rejections under 35 USC 103 (a) are not

persuasive. New art rejections under 35 USC 101 are included in this Office Action.

9.1   As per the applicants' argument that "none of the cited art teach requesting a resource in

which a thread manager, which controls threads each forming an execution unit of a program,

makes a request for information about a hardware resource; none of the cited art teach allocating

information about a hardware resource relating to necessary hardware resources to the thread by

said resource manager every time the generated thread is executed simulating the operation of

said logical unit to be conducted up to the completion; and none of the cited art teach simulation

using information relating to necessary hardware resources", the Examiner respectfully

disagrees.

        The applicants have explained in their amendment on Page 14, Para 2 that resource

signifies "information about a hardware resource" as disclosed in the specification on Page 22,

Lines 8-11. Using this interpretation of the "information about hardware resource" to mean

same as "the resource", the Examiner takes the position that Emer teaches requesting and

allocating "information about a hardware resource". Emer states at CL2, L3-6 that SMT

processor selects instructions for execution from all threads; and the processor then dynamically

schedules machine resources among the instruction. The examiner interprets this to mean that a

thread manager makes a request for information about a hardware resource and allocating

information about a hardware resource relating to necessary hardware resources to the thread by

said resource manager.

        Emer et al. teaches requesting a resource in which a thread manager, which controls

threads each forming an execution unit of a program, makes a request for information about a

hardware resource (CL2, L3-6); allocating information about a hardware resource relating to

necessary hardware resources to the thread by said resource manager every time the generated

thread is executed simulating the operation of said logical unit to be conducted up to the

completion (CL2, L3-6; CL1, L10-21; Fig. 1 (c); CL1, L66 to CL2, L6); and simulation using

information relating to necessary hardware resources (CL2, L3-6).

Conclusion

10.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

571-272-3717. The examiner can normally be reached on Monday through Friday from

8:00 AM to 5:30 PM.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

        Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

        Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

/Kandasamy Thangavelu/
Examiner, Art Unit 2123
July 12, 2008